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EXAMINER	
THOMAS, SHANE M	

ART UNIT	PAPER NUMBER
2186	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/685,579	KURAFUJI, TAKASHI	
	Examiner	Art Unit	
	Shane M. Thomas	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office action is responsive to the amendment filed 6/9/2006. Claims 1-7 and 15 are currently pending as claims 8-14 have been canceled. Applicants' arguments and amendments to the claims have been carefully considered, but they are not persuasive and do not place the claims in condition for allowance. Accordingly, this action has been made FINAL.

All previously outstanding objections and rejections to the Applicant's disclosure and claims not contained in this Action have been respectfully withdrawn by the Examiner hereto.

Response to Amendment

The Examiner has modified the rejection of the claims based on the Chin reference to incorporate Applicant's amendment to independent claims 1 and 15. Claims 1,2,4-7 and 15 remain rejected under 35 U.S.C. §102(b) as being anticipated by Chin (with supporting inherent teachings from Ghosh), and claim 3 remains rejected under 35 U.S.C. §103(a) as being unpatentable over Chin in view of Shiell. Specifically, the Examiner has redefined how he is interpreting a "cache memory device" such that the "cache memory device" does not incorporate the section of the motherboard that transmits the "buddy line signal" that indicates a second cache card is present in the system of Chin.

Specification

The disclosure is objected to because of the following informalities: the Examiner recommends amending the term --peculiar-- (page 44, lines 6 and 15) to --unique-- as suggested in the prior Office action.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1,2,4-7, and 1 5 are rejected under 35 U.S.C. 102(b) as being anticipated by Chin et al. (U.S. Patent No. 5,678,01 8). Further, the prior art reference of Ghosh et al. (U.S. Patent Application Publication No. 2002/0069333) is used for inherent teachings not disclosed or taught by Chin et al.

As per claim l, Chin teaches a **cache memory device** (L2 cache 200 - figure 2) that comprises **at least one cache memory** TAG and DATA RAMs 220 and 222 of each cache card 214,216 shown in figure 2 and **storing copy data of a main memory** (i.e. RAM memory) in (2/23-33). Further Chin teaches **a bank control circuit** (controller 218) **connected to at least one cache memory** (via buses shown between 218 and 220,222) **and capable of generating a plurality of control signals** (all internal control signals generated within the controller logic as shown in figure 4 for example) **for access to said at least one cache memory**. The **bank**

control circuit 218 **receives a signal indicative of cache capacity** (buddy line indication that determines whether a second cache card is installed on the system (2/34-36) and (3/7-15)) **from outside the cache memory device** 200 (from motherboard - (3/6-31)). **One control signal** (signal of address bit 21 - figure 4) **selected from the plurality of control signals** (all internal control signals of figure 4) is used to **access said at least one cache memory, respectively in accordance with said cache capacity signal** (buddy line) as taught in (3/7-31). Chin teaches accessing the data portion of the cache on card 214 or 216 when the control signal of address bit 21 is '0' or t 1 ' respectively. The signal carrying the logic of address bit 21 is being considered to be a control signal that is generated by the bank circuit 200 since the address bit signal 21 is latched by bank control circuit latch 416 as shown in figure 4; thus, the "BIT 21" signal was essentially generated by the bank control circuit as the logic of the address bit 21 was latched therein.

As per claim 2, the **bank control circuit** 200 **controls access to said at least one cache memory in such a manner that one accessing operation implements access to only one out of said at least one cache memory** as taught in (3/11-14) where, depending on the control signal of address bit 21 , only one of the caches on cards 214 and 2 16 are accessed. As taught in (3/31-50) and shown in figure 4, the proper signals must be active for bank control circuit logic to enable access to its respective cache.

As per claim 4, Chin teaches in figure 3 and (2/45-59) **cache address** bits 3-29 **indicating an address of main memory** bits 0-31 **and including a tag** bits 29-22 **and an index** bits 5-20 **are input to said cache memory device** (figure 1 , 200). **A bit position occupied by said tag and index is fixed in said cache address** is taught by Chin since the bit

position of the tag and index do not change based on the number of L2 cache cards present in the system (figure 3). The **at least one cache memory** of cards 214 and 21 6 each have a **tag memory**) 220 and **sets the index in the cache address to be an address** by which the tag memory 220 is accessed - (2/55-57). The **tag memory stores said tag of said cache address by** storing cache address bits 2 l -29 in the tag RAM 220 (2/57-59).

Chin teaches a **cache peripheral circuit** (which could a combination of the bank control circuit 218's latch 416 and logic required for generating a copy back address [to be discussed below] - for instance since latch 416 acquires the Master/Not Master signal to determine whether or not the current bank control circuit should access its respective cache based on the presence of other cache cards as well as the currently accessed memory location, of which the **index** is a part of that **links the index of the cache address input to the cache memory device when one or more cache memories accessed with at least one control signal selected by the bank control circuit** (as discussed supra) **is accessed, to data in the tag memory stored in the address indicated by the index** as well known in the caching art and shown in figure 3 and taught in (2/52-59). Further, **the cache peripheral circuit generates and outputs a copy back address** (via the bi-directional address bus as shown in figure 2) as part of the inherent copy-back (or write-back) scheme that is employed by the system of figure 1. A copy-back scheme (or write-back scheme as also referred to in the art) is known in the art to be a method of writing back data from the cache to the main memory. Chin teaches that the system of figure 1 is an arrangement of a Pentium™ microprocessor and Ghosh et al. teaches that Pentium™ caches use a write-back (copy-back) scheme (¶l5). Additionally, Chin specifically teaches in (4/4-22) that flushed of the 1.2 cache may occur as well. The term "flushing" is known in the art to be associated with write-

back (copy-back) caching; when a flush occurs, modified data is written from the cache back to main memory. Therefore, since the system of Chin implements a copy-back scheme for updating main memory data, the cache peripheral circuit (as defined above) must therefore generate and output the address of the modified data stored in the data caches of cards 214 and 216 in order to modify the correct locations of main memory (i.e. the copy-back addresses).

Therefore, as discussed above, it can be seen that the system of Chin employs a **copy back method using the copy back address as a writing method for main memory**.

As per claim 5, the rejection of lines 1 -7 follows the rejection for claim 4, lines 1-7, discussed supra. Regarding the remainder of claim 5, Chin teaches a **comparator** 314 **for comparing the tag in the cache address input to the cache memory device when one or more cache memories accessed with said at least one control signal selected by said bank control circuit** (as discussed supra) **is accessed, to data in the tag memory stored in the address indicated by the index in said cache address and for detecting their coincidence/no-coincidence** - (2/52-64).

As per claim 6, the **at least one cache memory** 116 of Chin actually can have a **plurality of cache memories** (comprised on cards 214 and 216 as shown in figure 2 and taught in 2/34-44). Chin teaches in figure 3 and (2/45-59) a **cache address** bits 3-29 **indicating an address of main memory** bits 0-31 **and including a tag** bits 29-22 **and an index** bits 5-**20 is input to said cache memory device** (figure l, 200). A **bit position occupied by said tag and index is fixed in said cache address** is taught by Chin since the bit position of the tag and index do not changed based on the number of L2 caches present in the system (figure 3).

The **plurality of cache memories have respective tag memories for storing the tag of the cache address** as taught in (2/34-44). Chin teaches that the **respective tag memories** 220 **store plural pieces of fixed data unique to said plurality of cache memories, respectively** because each tag RAM 220 of cache 214 or 2l6 can only store the data corresponding to whether the control signal of the address bit 21 is active, meaning that for cache addresses which have address bit 2 1 set as '0', the cache RAMs on card 214 will be accessed whereas if the address bit 21 is set as '1', the cache RAMs on card 21 6 will be accessed - (3/11 -14). Thus, it can be seen (figure 3) that depending on the address bit 2l of the incoming address, the plural fixed data pieces (fixed because the number of tag bits never change as discussed supra) are stored in the plurlaity of tag memories. **Each of the plural pieces of fixed data** (i.e. bits 22-29 of the incoming address previously stored in Tag RAM 312) **correspond to a part of the tag** since the Tag RAM 3 l 2 stores every part of the incoming tag as known in the art and shown in figure 3.

As per claim 7, **the at least one cache memory** 116 of Chin actually can have a **plurality of cache memories** (comprised on cards 214 and 21 6 as shown in figure 2 and taught in 2/34-44). The **plurality of cache memories have the same memory capacity** since each of the memory cards comprising the cache lkAMs of Chin are identical (2/34-44).

As per claim 15, Chin teaches a **bank control circuit** 200 **controlling access to a cache memory** (combination of the caches on cards 214 and 216) **that comprises a decoder** (combination of the logic portion of the controllers 218 of the cards 214 and 216 that is shown in figure 4) **receiving first and second signals from outside a cache memory device** (buddy line signal [discussed in the rejection of figure 1 as being received from motherboard - 3/15-30]

indicating more than one cache card is installed on the bank control circuit 200 and BIT 21 [as obtained outside the cache memory device 116 from the buses 110 and 112 as shown in figure 2] signal of incoming cache address as shown in figure 4, respectively) **and outputting bank select signals** (each controller outputs the signal result of OR gate 412 in order to activate its respective cache - 3/32-50) **such that one of the bank select signals is active in accordance with said first and second signals** (as shown in figure 4 and taught in 3/11 -50), the bank control signal - result of OR gate 42 - for the "master" card 214 cache is active when the first signal is inactive '0' and the second signal is active '1' and the bank select signal for the "slave" card 216 cache is active when both the first and second signals are inactive '0') **wherein said first signal is indicative of a cache capacity used in the cache memory** (the buddy line produces a signal that is latched by latch 416 to produce SINGLE signal (figure 4 and 3/16-22), which designates whether one or two caches are present in the system of Chin - (3/43/46)) **and the second signal is a part of an address supplied to the cache memory** (BIT 21 is the 21St bit of an incoming cache address - (3/7-15)).

Further, Chin teaches **signal output circuits** (the portion of the controller 218 that actually sends data to and from the tag ram 220 and data ram 222 via the buses shown on figure 2) **provided correspondingly to the bank select signals, respectively** since in order for the signal output circuits to forward information received from the address/control bus 112 and data bus 110, the bank select signal (output of respective OR gate 412) must be active (3/41-50). **Each signal output circuit receives a control signal for accessing the cache memory** (one of control signals shown in figure 2 being transmitted between the controllers 218 and the bus 110 or any address signal that could be transmitted to the tag or data RAMs from the bus 110) **and a**

corresponding bank select signal (since the output of the OR gate 412 is needed in order to determine whether or not the respective tag and data RAMs will be accessed) and **permitting the control signal to be output to the cache memory in response to an active state of said corresponding bank select signal** (data is forwarded to the RAMs when the respective bank select circuit is active - (3/41-50)) **while inhibiting said control signal to be output to the cache memory in response to a non-active state of said corresponding bank select signal** (likewise it can be inferred such that when the output of the OR gate 412 is inactive, the corresponding RAMs are not accessed - (3/41/50)).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chin et al. (U.S. Patent No. 5,678,018) in view of Shiell et al. (U.S. Patent No. 6,442,667).

As per claim 3, the **at least one cache memory** 1 16 of Chin actually can have a **plurality of cache memories** (comprised on cards 214 and 216 as shown in figure 2 and taught in 2/34-44). Further, Chin teaches that depending on the incoming address bit 21 that only one of the two caches on cards 214 and 216 are accessed (3/1 1-14). As it is well known in the art that caching components require power to operate, **a power control circuit** (i.e. a portion of the motherboard that controls power to the plurality of caches on cards 214 and 216 - probably via

the motherboard connectors 210 and 212 (2/34-36)) **for controlling power supply to the plurality of cache memories connected to the bank control circuit based on said signal** is an inherent component of the motherboard since only the first cache would be supplied power when there is only one cache card 214 installed and when the second or slave card comprising the second L2 cache is installed, and the buddy line signal inactive. It would have been seen that the second cache would have been supplied with power as well, thereby enabling the CPU 120 the ability to access the second 1.2 cache. However, Chin does not specifically teach the cache memory device of figure 2 further comprising **a power control circuit supplying power to one or more cache memories accessed with said at least one control signal selected by said bank control circuit out of the plurality of cache memories**. In other words, Chin does not teach supplying power to only the cache memory 214 or 216 which currently needs to be accessed (i.e. bit 21 of the incoming address) by a cache request.

Shiell teaches a method to only power a portion of an L2 cache memory based on translated (i.e. decoded address bits) (7/21-23) and (9/6-10). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have combined the selective caching system of Chin with the teaching of selectively supplying of power to only the portion of the cache that is currently being accessed of Shiell in order to have gained reduced the overall power dissipation of the combined 1.2 cache (214, 216). It could have been seen that since the controllers 218 receive the address from buses 110 and 112, that the controller portion of the cache memory device could have

determined whether or not to supply power to its respective tag and data RAM arrays based on the decoded address. One having ordinary skill in the art would have seen that such a modification to the system of Chin would have yielded immediate benefits. By using translated bits of the incoming address (namely address bit 21), modified Chin would have been able to not only select which cache was to perform the requested read or write access, but with the teaching of Shiell, would have been able to supply power to only that respective cache (214, 216), thereby conserving the power that would have been required to operate the other cache card not being accessed when it would not have been required to have been accessed.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane M. Thomas whose telephone number is (571) 272-4188. The examiner can normally be reached on M-F 8:30 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt M. Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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